DIGITALS ELECTRONICS IMPORTANT MCQ WITHSOLUTION

Q.1 The NAND gate output will be low if the two inputsare

(A)00 **(B)**01
(C)10 **(D)**11

Ans: D

The NAND gate output will be low if the two inputs are 11
(The Truth Table of NAND gate is shown in Table.1.1)

X(Input)	Y(Input)	F(Output)
0	0	1
0	1	1
1	0	1
1	1	0

Table 1.1 Truth Table for NAND Gate

Q.2 Whatisthebinaryequivalentofthedecimalnumber368

(A)101110000 **(B)**110110000
(C)111010000 **(D)**111100000

Ans: A

The Binary equivalent of the Decimal number 368 is 101110000
(Conversion from Decimal number to Binary number is given in Table 1.2)

2	368
2	184 --- 0
2	92 ---0
2	46 ---0
2	23 ---0
2	11 ---1
2	5 ---1
2	2 ---1
2	1 ---0
	0 --- 1

Table 1.2 Conversion from Decimal number to Binary number

Q.3 The decimal equivalent of hex number 1A53is

(A)6793 **(B)**6739

(C)6973 **(D)**6379

Ans: B

The decimal equivalent of Hex Number 1A53 is 6739

(Conversion from Hex Number to Decimal Number is given below)

1	A	5	3	Hexadecimal
16^3	16^2	16^1	16°	Weights

$(1A53)_{16} = (1X16^3) + (10 X 16^2) + (5 X 16^1) + (3 X 16^o)$

$=4096 + 2560 + 80 + 3$

$= 6739$

Q.4 $(734)_8 = ()_{16}$

(A) C 1 D **(B)** D C1

(C) 1C D **(D)** 1 DC

Ans: D

$(734)_8 = (1\ DC)_{16}$

0001 | 1101 | 1100

1 D C

Q.5 The simplification of the Boolean expression $\left(ABC\right)+\left(ABC\right)$ is

(A)0 **(B)**1

(C)A **(D)**BC

Ans: B

The Boolean expression is $\left(ABC\right) + A\left(BC\right)$ is equivalent to 1

$\left(ABC\right)+\left(ABC\right)=A+B+C\overline{+}A+B+C\overline{=}A+B+\overline{C}+A+B+\overline{C}$

$= (A+\overline{A})(B+\overline{B})(C+\overline{C}) = 1X1X1 = 1$

Q.6 The number of control lines for a 8 – to – 1 multiplexeris

(A)2 **(B)**3

(C)4 **(D)**5

Ans: B

The number of control lines for an 8 to 1 Multiplexer is 3

(The control signals are used to steer any one of the 8 inputs to the output)

Q.7 How many Flip-Flops are required for mod–16counter?

(A)5 **(B)**6

(C)3 **(D)**4

Ans: D

The number of flip-flops is required for Mod-16 Counter is 4.

(For Mod-m Counter, we need N flip-flops where N is chosen to be the smallest number for which 2N is greater than or equal to m. In this case 24 greater than or equal to 1)

Q.8 EPROM contents can be erased by exposing itto

(A) Ultravioletrays. **(B)** Infraredrays.
(C) Burstofmicrowaves. **(D)** Intense heatradiations.

Ans: A

EPROM contents can be erased by exposing it to Ultraviolet rays
(The Ultraviolet light passes through a window in the IC package to the EPROM chip where it releases stored charges. Thus the stored contents areerased).

Q.9 Thehexadecimalnumber'A0'hasthedecimalvalueequivalentto

(A) 80 **(B)**256
(C) 100 **(D)**160

Ans: D

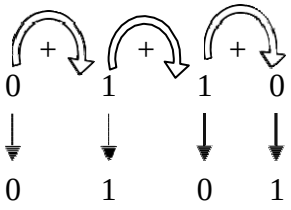
Thehexadecimalnumber'A0'hasthedecimalvalueequivalentto160 (A
0
16^1 16^0 = 10X16^1 + 0X16^0 = 160)

Q.10 The Gray code for decimal number 6 is equivalentto

(A)1100 **(B)**1001
(C)0101 **(D)**0110

Ans: C

The Gray code for decimal number 6 is equivalent to 0101
(Decimal number 6 is equivalent to binary number 0110)



Q.11 The Boolean expression $\overline{A}$.B + A.$\overline{B}$ + A.B is equivalentto

(A) A +B **(B)**$\overline{A}$.B
(C) $\overline{A+B}$ **(D)**A.B

Ans:A

The Boolean expression $\overline{A}$ .B + A. $\overline{B}$ + A.B is equivalent to A + B
($\overline{A}$ .B + A. $\overline{B}$ + A.B = B($\overline{A}$ + A) + A. $\overline{B}$
= B + A. $\overline{B}$ { ($\overline{A}$ + A) = 1}
= A + B **{** (B + A. $\overline{B}$) = B + A}

Q.12 The digital logic family which has minimum power dissipationis

(A) TTL **(B)**RTL
(C)DTL **(D)**CMOS

Ans:D

The digital logic family which has minimum power dissipation is CMOS.
(CMOS being an unipolar logic family, occupy a very small fraction of silicon Chip area)

Q.13 Theoutputofalogic gateis1whenallitsinputsareatlogic0.thegateiseither
(A) a NAND oranEX-OR **(B)** an OR or anEX-NOR
(C) an AND oranEX-OR **(D)** a NOR or anEX-NOR

Ans:D

The output of a logic gate is 1 when all inputs are at logic 0. The gate is either a NOR or an EX-NOR .

(The truth tables for NOR and EX-NOR Gates are shown in fig.1(a) & 1(b).)

Input		Output
A	**B**	**Y**
0	0	1
0	1	0
1	0	0
1	1	0

Fig.1(a) Truth Table for NOR Gate

Input		Output
A	**B**	**Y**
0	0	1
0	1	0
1	0	0
1	1	1

Fig.1(b) Truth Table for EX-NOR Gate

Q.14 Data can be changed from special code to temporal codebyusing
(A) Shiftregisters **(B)**counters
(C) Combinationalcircuits **(D)** A/Dconverters.

Ans:A

DatacanbechangedfromspecialcodetotemporalcodebyusingShiftRegisters. (A Register in which data gets shifted towards left or right when clock pulses are applied is known as a ShiftRegister.)

Q.15 AringcounterconsistingoffiveFlip-Flopswillhave
(A) 5states **(B)** 10states
(C)32states **(D)** Infinitestates.

Ans:A

A ring counter consisting of Five Flip-Flops will have 5 states.

Q.16 The speed of conversion is maximumin
(A) Successive-approximation A/Dconverter.
(B) Parallel-comparative A/Dconverter.
(C) Counter ramp A/Dconverter.
(D) Dual-slope A/Dconverter.

Ans:B

The speed of conversion is maximum in Parallel-comparator A/D converter
(Speed of conversion is maximum because the comparisons of the input voltage are carried out simultaneously.)

Q.17 The 2's complement of the number 1101101is

(A)0101110 **(B)**0111110
(C)0110010 **(D)**0010011

Ans:D

The 2's complement of the number 1101101 is 0010011
(1's complement of the number 1101101 is 0010010
2's complement of the number 1101101is 0010010 + 1 =0010011)

Q.18 Thecorrectiontobeappliedindecimaladdertothegeneratedsumis

(A)00101 **(B)**00110
(C)01101 **(D)**01010

Ans:B

The correction to be applied in decimal adder to the generated sum is 00110.
When the four bit sum is more than 9 then the sum is invalid. In such cases, add +6(i.e. 0110) to the four bit sum to skip the six invalid states. If a carry is generated when adding 6, add the carry to the next four bit group.

Q.19 When simplified with Boolean Algebra (x + y)(x + z) simplifiesto

(A) x **(B)** x + x(y +z)
(C) x(1+yz) **(D)** x +yz

Ans:D

When simplified with Boolean Algebra (x + y)(x + z) simplifies to x + yz
[(x + y) (x + z)] = xx + xz + xy + yz = x + xz + xy +yz(xx =x)
= x(1+z) + xy + yz = x + xy +yz{ (1+z) =1}
= x(1 + y) + yz = x +yz{ (1+y) =1}]

Q.20 The gates required to build a half adderare

(A) EX-OR gate andNORgate **(B)** EX-OR gate and ORgate
(C) EX-OR gate andANDgate **(D)** Four NANDgates.

Ans:C

The gates required to build a half adder are EX-OR gate and AND gate
Fig.1(d) shows the logic diagram of half adder.

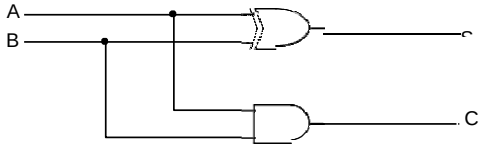


Fig.1(d) Logic diagram of Half Adder

Q.21 Thecodewhereallsuccessivenumbersdifferfromtheirprecedingnumberbysinglebitis

(A) Binarycode. **(B)**BCD.
(C) Excess–3. **(D)**Gray.

Ans:D

The code where all successive numbers differ from their preceding number by single bit is Gray Code.
(It is an unweighted code. The most important characteristic of this code is that only a single bit change occurs when going from one code number to next.)

Q.22 Which of the following is the fastestlogic

(A) TTL **(B)**ECL
(C)CMOS **(D)**LSI

Ans:B

ECL is the fastest logic family of all logic families.
(High speeds are possible in ECL because the transistors are used in difference amplifier configuration, in which they are never driven into saturation and thereby the storage time iseliminated.

Q.23 If the input to T-flipflop is 100 Hz signal, the final output of the three T-flipflops in cascadeis

(A)1000Hz **(B)** 500Hz
(C)333Hz **(D)** 12.5Hz.

Ans:D

If the input to T-flip-flop is 100 Hz signal, the final output of the three T- flip-flops in cascade is 12.5Hz

{The final output of the three T-flip-flops in cascade is

$(T) = \frac{Frequency}{2^N} = \frac{100}{2^3} = 12.5Hz\}$

Q.24 Which of the memory is volatilememory

(A) ROM **(B)**RAM
(C)PROM **(D)**EEPROM

Ans:B

RAM is a volatile memory
(Volatile memory means the contents of the RAM get erased as soon as the power goes off.)

Q.25 -8 is equal to signed binarynumber

(A)10001000 **(B)**00001000
(C)10000000 **(D)**11000000

Ans:A

- 8 is equal to signed binary number 10001000

(To represent negative numbers in the binary system, Digit 0 is used for the positive sign and 1 for the negative sign. The MSB is the sign bit followed by the magnitude bits.i.e.,

- 8 = 10001000

Sign Magnitude

Q.26 DeMorgan's first theorem shows the equivalenceof

(A) OR gate and Exclusive ORgate.
(B) NOR gate and Bubbled ANDgate.
(C) NOR gate and NANDgate.
(D) NAND gate and NOTgate

Ans:B

DeMorgan's first theorem shows the equivalence of NOR gate and Bubbled AND gate

(Logic diagrams for De Morgan's First Theorem is shown in fig.1(a)

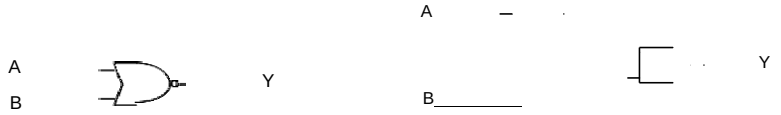


Fig.1(a) Logic Diagrams for De Morgan's First Theorem

Q.27 The digital logic family which has the lowest propagation delaytimeis

(A) ECL **(B)** TTL
(C) CMOS **(D)** PMOS

Ans:A

The digital logic family which has the lowest propagation delay time is ECL

(Lowest propagation delay time is possible in ECL because the transistors are used in difference amplifier configuration, in which they are never driven into saturation and thereby the storage time is eliminated).

Q.28 The device which changes from serial data to parallel datais

(A) COUNTER **(B)** MULTIPLEXER
(C)DEMULTIPLEXER **(D)** FLIP-FLOP

Ans:C

The device which changes from serial data to parallel data is demultiplexer.

(A demultiplexer takes in data from one line and directs it to any of its N outputs depending on the status of the select inputs.)

Q.29 A device which converts BCD to Seven Segment iscalled

(A) Encoder **(B)** Decoder
(C) Multiplexer **(D)** Demultiplexer

Ans:B

A device which converts BCD to Seven Segment is called DECODER.

(A decoder coverts binary words into alphanumeric characters.)

Q.30 In a JK Flip-Flop, togglemeans

(A) Set Q = 1 and $\overline{Q}$ =0.

(B) Set Q = 0 and $\overline{Q}$ =1.

(C) Change the output to the oppositestate.

(D) No change inoutput.

Ans:C

In a JK Flip-Flop, toggle means Change the output to the opposite state.

Q.31 The access time of ROM using bipolar transistors isabout

(A) 1sec **(B)** 1msec

(C)1µsec **(D)** 1nsec.

Ans:C

The access time of ROM using bipolar transistors is about 1 μsec.

Q.32 TheA/Dconverterwhoseconversiontimeisindependentofthenumberofbitsis

(A) Dualslope **(B)** Countertype

(C) Parallelconversion **(D)** Successiveapproximation.

Ans:C

The A/D converter whose conversion time is independent of the Number of bits is Parallel conversion.

(This type uses an array of comparators connected in parallel and comparators compare the input voltage at a particular ratio of the reference voltage).

Q.33 When signed numbers are used in binary arithmetic, then which one of the following notations would have unique representation forzero.

(A) Sign-magnitude. **(B)** 1'scomplement.

(C) 2'scomplement. **(D)** 9'scomplement.

Ans: A

Q.34 The logic circuit given below (Fig.1) converts a binarycode y_1y_2 $y_3$into

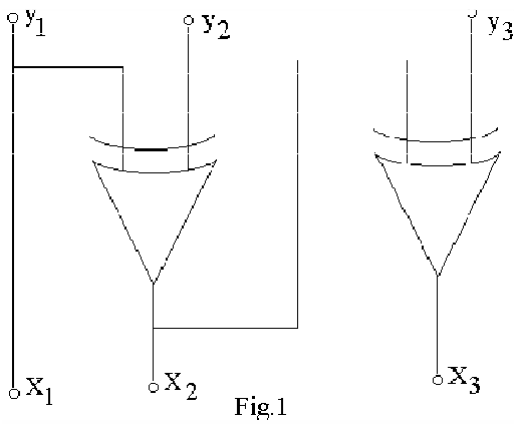


Fig.1

(A) Excess-3code. **(B)** Graycode.
(C) BCD code. **(D)** Hamming code.

Ans: B

Gray code as

X1=Y1, X2=Y1 XOR Y2 , X3=Y1 XOR Y2 XORY3

For	Y1	Y2	Y3	X1	X2	X3
	0	0	0	0	0	0
	0	0	1	0	0	1
	0	1	0	0	1	1
	0	1	1	0	1	0

Q.35 The logic circuit shown in the given fig.2 can be minimisedto

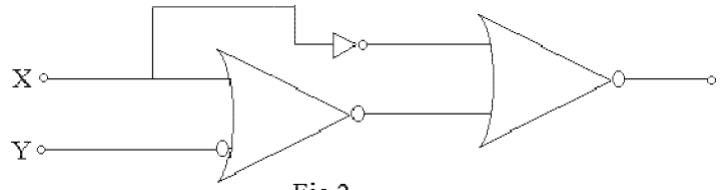
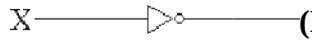
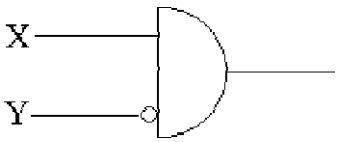
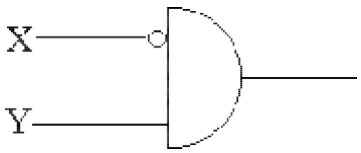
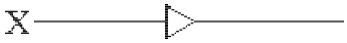


Fig.2

(A) 

(B) 

(C) 

(D) 

Ans: D

As output of the logic circuit is
Y=(X+Y')'+(X'+(X+Y')')'
(X+Y')'=X'Y Using DE Morgan's
Now this is one of input of 2nd gate. F=(A+X')'=A'X=[(X'Y)'.X]
=[(X+Y')X]=X+XY'=X(Y')
=X

Q.36 IndigitalICs,Schottkytransistorsarepreferredovernormaltransistorsbecauseoftheir

(A) LowerPropagationdelay. **(B)** Higher Propagationdelay.
(C) LowerPowerdissipation. **(D)** Higher Powerdissipation.

Ans: A

Lower propagation delay as shottky transistors reduce the storage time delay by preventing the transistor from going deep into saturation.

Q.37 Thefollowingswitchingfunctionsaretobeimplementedusinga Decoder:

$f_1=\sum m(1, 2, 4, 8, 10, 14)\ f_2=\sum m(2, 5, 9, 11)\ f_3=\sum m(2, 4, 5, 6, 7)$

The minimum configuration of the decoder should be

(A) 2 – to –4line. **(B)** 3 – to – 8line.
(C) 4 – to –16line. **(D)** 5 – to – 32line.

Ans: C

4 to 16 line decoder as the minterms are ranging from 1 to 14.

Q.38 A 4-bit synchronous counter uses flip-flops with propagation delay times of 15 ns each. The maximum possible time required for change of state willbe

(A)15ns. **(B)** 30ns.
(C)45ns. **(D)** 60ns.

Ans: A

15 ns because in synchronous counter all the flip-flops change state at the same time.

Q.39 Words having 8-bits are to be stored into computer memory. The number of lines requiredfor writing into memoryare

(A)1. **(B)**2.
(C)4. **(D)**8.

Ans: D

Because 8-bit words required 8 bit data lines.

Q.40 In successive-approximation A/D converter, offset voltage equalto $\frac{1}{2}$LSB is added to the D/A converter's output. This is doneto

(A) Improve the speed ofoperation.
(B) Reduce the maximum quantizationerror.
(C) Increase the number of bits at theoutput.
(D) Increasetherangeofinputvoltagethat canbeconverted.

Ans: B

Q.41 The decimal equivalent of Binary number 11010is

(A)26. **(B)**36.
(C) 16. **(D)**23.

Ans: A

$11010 = 1 \text{ X } 2^4 + 1 \text{ X } 2^3 + 0 \text{ X } 2^2 + 1 \text{ X } 2^1 = 26$

Q.42 1'scomplementrepresentationofdecimalnumberof-17byusing8bitrepresentationis

(A)11101110 **(B)** 11011101
(C)11001100 **(D)** 00010001

Ans: A

$(17)_{10} = (10001)_2$
In 8 bit = 00010001
1's Complement = 11101110

Q.43 The excess 3 code of decimal number 26is

(A)01001001 **(B)**01011001
(C)10001001 **(D)**01001101

Ans: B

$(26)_{10}$ in BCD is (00100110) BCD
Add 011 to each BCD 01011001 for excess – 3

Q.44 How many AND gates are required to realize Y =CD+EF+G

(A)4 **(B)**5
(C)3 **(D)**2

Ans: D

To realize Y = CD + EF + G
Two AND gates are required (for CD & EF).

Q.45 How many select lines will a 16 to 1 multiplexer willhave

(A)4 **(B)**3
(C)5 **(D)**1

Ans: A

In 16 to 1 MUX four select lines will be required to select 16 (2^4) inputs.

Q.46 How many flip flops are required to construct a decadecounter

(A)10 **(B)**3
(C)4 **(D)**2

Ans: C

Decade counter counts 10 states from 0 to 9 (i.e. from 0000 to 1001)
Thus four FlipFlop's are required.

Q.47 Which TTL logic gate is used for wiredANDing

(A) Opencollectoroutput **(B)** TotemPole
(C) Tristateoutput **(D)** ECLgates

Ans: A

Open collector output.

Q.48 CMOS circuits consumepower

(A) Equalto TTL **(B)** Less thanTTL
(C) TwiceofTTL **(D)** Thrice ofTTL

Ans: B

As in CMOS one device is ON & one is Always OFF so power consumption is low.

Q.49 In a RAM, information can bestored

(A) By the user, number oftimes.

(B) By the user, onlyonce.
(C) By the manufacturer, a number oftimes.
(D) By the manufacturer onlyonce.

Ans: A

RAM is used by the user, number of times.

Q.50 The hexadecimal number for $(95.5)_{10}$ is

(A) $(5F.8)_{16}$ **(B)** $(9A.B)_{16}$

(C) $(2E.F)_{16}$ **(D)** $(5A.4)_{16}$

Ans: A

$(95.5)_{10} = (5F.8)_{16}$

Integerpart

16 | 95
16 | 5 — 15 ↑
0 — 5

Fractionalpart

0.5x16=8.0

Q.51 The octal equivalent of $(247)_{10}$is

(A) $(252)_8$ **(B)** $(350)_8$

(C) $(367)_8$ **(D)** $(400)_8$

Ans: C

$(247)_{10} = (367)_8$

8 | 247
8 | 30 — 7 ↑
8 | 3 — 6
0 — 3

Q.52 Thechiefreasonwhydigitalcomputersusecomplementedsubtractionisthatit

(A) Simplifies thecircuitry.
(B) Is a very simpleprocess.
(C) Can handle negative numberseasily.
(D) Avoids directsubtraction.

Ans: C

Using complement method negative numbers can also be subtracted.

Q.53 In a positive logic system, logic state 1 correspondsto

(A) positivevoltage **(B)** higher voltagelevel
(C) zerovoltagelevel **(D)** lower voltagelevel

Ans: B

We decide two voltages levels for positive digital logic. Higher voltage represents logic 1 & a lower voltage represents logic 0.

Q.54 Thecommerciallyavailable8-inputmultiplexerintegratedcircuitintheTTLfamilyis

(A)7495. **(B)**74153.
(C)74154. **(D)**74151.

Ans: B

MUX integrated circuit in TTL is 74153.

Q.55 CMOScircuitsareextensivelyusedforON-chipcomputersmainlybecauseoftheirextremely

(A) lowpowerdissipation. **(B)** high noiseimmunity.
(C) largepackingdensity. **(D)** lowcost.

Ans: C

Because CMOS circuits have large packing density.

Q.56 The MSI chip 7474is

(A) Dual edge triggered JK flip-flop(TTL).
(B) Dual edge triggered D flip-flop(CMOS).
(C) Dual edge triggered D flip-flop(TTL).
(D) Dual edge triggered JK flip-flop(CMOS).

Ans: C

MSI chip 7474 dual edge triggered D Flip-Flop.

Q.57 Which of the following memories stores the most number ofbits

(A) a 5M×8memory. **(B)** a 1M × 16memory.
(C) a 5M ×4memory. **(D)** a 1M ×12memory.

Ans: A

5Mx8 = 5 x 220 x 8 = 40M (max)

Q.58 The process of entering data into a ROM iscalled

(A) burning intheROM **(B)** programming theROM
(C) changingtheROM **(D)** charging theROM

Ans: B

The process of entering data into ROM is known as programming the ROM.

Q.59 Whenthesetofinputdatatoanevenparitygeneratoris0111,theoutputwillbe

(A)1 **(B)**0
(C) Unpredictable **(D)** Depends on the previousinput

Ans: B

In even parity generator if number of 1 is odd then output will be zero.

Q.60 The number 140 in octal is equivalentto

(A) $(96)_{10}$. **(B)** $(86)_{10}$.

(C) $(90)_{10}$. **(D)** none ofthese.

Ans: A

$(140)_8 = (96)_{10}$

$1 \times 8^2 + 4 \times 8 + 0 \times 1 = 64 + 32 = 96$

Q.61 The NOR gate output will be low if the two inputsare

(A)00 **(B)**01

(C)10 **(D)**11

Ans: B, C, or D

O/P is low if any of the I/P is high

Q.62 Which of the following is the fastestlogic?

(A) ECL **(B)**TTL

(C)CMOS **(D)**LSI

Ans: A

Q.63 How manyflip-flops are required to construct mod 30counter

(A)5 **(B)**6

(C)4 **(D)**8

Ans: A

Mod - 30 counter +/- needs 5 Flip-Flop as $30 < 2^5$

Mod - N counter counts total ' N ' number of states.

To count 'N' distinguished states we need minimum n FlipFlop's as [$N = 2^n$]

For eg. Mod 8 counter requires 3 Flip-Flop's ($8 = 2^3$)

Q.64 How many address bits are required to represent a 32 Kmemory

(A) 10bits. **(B)** 12bits.

(C)14bits. **(D)** 16bits.

Ans: D

$32K = 2^5 \times 2^{10} = 2^{15}$,

Thus 15 address bits are required, Only 16 bits can address it.

Q.65 The number of control lines for 16 to 1multiplexeris

(A)2. **(B)**4.

(C)3. **(D)**5.

Ans: B

As $16 = 2^4$, 4 Select lines are required.

Q.66 Which of following requiresrefreshing?

(A) SRAM. **(B)**DRAM.

(C)ROM. **(D)**EPROM.

Ans: B

Q.67 Shiftingaregistercontenttoleftbyonebitpositionisequivalentto
(A) divisionbytwo. **(B)** addition bytwo.
(C) multiplicationbytwo. **(D)** subtraction bytwo.

Ans:C

Q.68 ForJKflipflopwithJ=1,K=0,theoutputafterclockpulsewillbe
(A)0. **(B)**1.
(C)highimpedance. **(D)** nochange.

Ans: B

Q.69 Convert decimal 153 to octal. Equivalent in octal willbe
(A) $(231)_8$. **(B)**$(331)_8$.
(C) $(431)_8$. **(D)** none ofthese.

Ans: A
$(153)_{10} = (231)_8$

8	153	1
8	19	3
8	2	2

Q.70 The decimal equivalent of $(1100)_2$is
(A)12 **(B)**16
(C)18 **(D)**20

Ans: A
$(1100)_2 = (12)_{10}$

Q.71 The binary equivalent of $(FA)_{16}$is
(A)10101111 **(B)** 11111010
(C)10110011 **(D)** none ofthese

Ans: B
$(FA)_{16} = (11111010)_{10}$

Q.72 The output of SR flip flop when S=1, R=0is
(A)1 **(B)**0
(C) Nochange **(D)** Highimpedance

Ans: A

As for the SR flip-flop S=set input R=reset input ,when S=1, R=0, Flip-flop will be set.

Q.73 The number of flip flops contained in IC 7490is

(A)2. **(B)**3.
(C)4. **(D)**10.

Ans: A

Q.74 The number of control lines for 32 to 1multiplexeris

(A)4. **(B)**5.
(C)16. **(D)**6.

Ans: B

The number of control lines for 32 (2^5) and to select one input among them total 5 select lines are required.

Q.75 HowmanytwO-inputANDandORgatesarerequiredtorealizeY=CD+EF+G

(A)2,2. **(B)**2,3.
(C)3,3. **(D)** none ofthese.

Ans: A

Y=CD+EF+G
Number of two input AND gates=2
Number of two input OR gates = 2
One OR gate to OR CD and EF and next to OR of G & output of first OR gate.

Q.76 Which of following can not be accessedrandomly

(A) DRAM. **(B)**SRAM.
(C)ROM. **(D)** Magnetictape.

Ans: D

Magnetic tape can only be accessed sequentially.

Q.77 The excess-3 code of decimal 7 is representedby

(A)1100. **(B)**1001.
(C)1011. **(D)**1010.

Ans: D

An excess 3 code is always equal to the binary code +3

Q.78 WhenaninputsignalA=11001isappliedtoaNOTgateserially,itsoutputsignalis

(A)00111. **(B)**00110.
(C)10101. **(D)**11001.

Ans: B

As A=11001 is serially applied to a NOT gate, first input applied will be LSB 00110.

Q.79 The result of adding hexadecimal number A6 to 3Ais

(A) DD. **(B)**E0.
(C)F0. **(D)**EF.

Ans: B

Q.80 A universal logic gate is one, which can be used to generate any logic function. Which of the following is a universal logicgate?

(A) OR **(B)**AND
(C)XOR **(D)**NAND

Ans: D

NAND can generate any logic function.

Q.81 The logic 0 level of a CMOS logic device isapproximately

(A) 1.2volts **(B)** 0.4volts
(C)5volts **(D)** 0volts

Ans: D

CMOS logic low level is 0 volts approx.

Q.82 Karnaugh map is used for the purposeof

(A) Reducing the electronic circuitsused.
(B) To map the given Boolean logicfunction.
(C) To minimize the terms in a Booleanexpression.
(D) To maximize the terms of a given a Booleanexpression.

Ans: C

Q.83 A full adder logic circuit willhave

(A) Two inputs and oneoutput.
(B) Three inputs and threeoutputs.
(C) Two inputs and twooutputs.
(D) Three inputs and twooutputs.

Ans: D

A full adder circuit will add two bits and it will also accounts the carry input generated in the previous stage. Thus three inputs and two outputs (Sum and Carry) are there.

Q.84 An eight stage ripple counter uses a flip-flop with propagation delay of 75 nanoseconds. The pulse width of the strobe is 50ns. The frequency of the input signal which can be used for proper operation of the counter isapproximately

(A) 1MHz. **(B)** 500MHz.
(C)2MHz. **(D)** 4MHz.

Ans: A

Maximum time taken for all flip-flops to stabilize is 75ns x 8 + 50 = 650ns. Frequency of operation must be less than 1/650ns = 1.5 MHz.

Q.85 The output of a JK flipflop with asynchronous preset and clear inputs is '1'. The output can be changed to '0' with one of the followingconditions.

(A) By applying J = 0, K = 0 and using aclock.
(B) By applying J = 1, K = 0 and using theclock.
(C) By applying J = 1, K = 1 and using theclock.
(D) By applying a synchronous presetinput.

Ans: C

Preset state of JK Flip-Flop =1
With J=1 K=1 and the clock next state will be complement of the present state.

Q.86 The information in ROM isstored

(A) By the user any number oftimes.
(B) By the manufacturer during fabrication of thedevice.
(C) By the user using ultravioletlight.
(D) By the user once and onlyonce.

Ans: B

Q.87 The conversation speed of an analog to digital converter is maximum with thefollowing technique.

(A) Dual slope ADconverter.
(B) Serial comparator ADconverter.
(C) Successive approximation ADconverter.
(D) Parallel comparator ADconverter.

Ans: D

Q.88 AweightedresistordigitaltoanalogconverterusingNbitsrequiresatotal of

(A) Nprecisionresistors. **(B)** 2N precisionresistors.
(C) N + 1precisionresistors. **(D)** N – 1 precisionresistors.

Ans: A

Q.89 The 2's complement of the number 1101110is

(A)0010001. **(B)**0010001.
(C)0010010. **(D)**None.

Ans: C

1's complement of 1101110 is = 0010001
Thus 2's complement of 1101110 is = 0010001 + 1 = 0010010

Q.90 The decimal equivalent of Binary number 10101is

(A)21 **(B)**31
(C)26 **(D)**28

Ans: A

$1x2^4 + 0x2^3 + 1x2^2 + 0x2^1 + 1x2^0$

$= 16 + 0 + 4 + 0 + 1 = 21.$

Q.91 How many two input AND gates and two input OR gates are required to realize Y =BD+CE+AB

(A) 1, 1 **(B)** 4,2

(C) 3, 2 **(D)** 2,3

Ans: A

There are three product terms, so three AND gates of two inputs are required.
As only two input OR gates are available, so two OR gates are required to get the logical sum of three product terms.

Q.92 How many select lines will a 32:1 multiplexer will have

(A) 5. **(B)** 8.

(C) 9. **(D)** 11.

Ans: A

For 32 inputs, 5 select lines will be required, as $2^5 = 32$.

Q.93 How many address bits are required to represent 4K memory

(A) 5bits. **(B)** 12bits.

(C) 8bits. **(D)** 10bits.

Ans: B

For representing 4K memory, 12 address bits are required as 4K

$= 2^2 \times 2^{10} = 2^{12}$ $(1K = 1024 = 2^{10})$

Q.94 For JK flip flop J = 0, K=1, the output after clock pulse will be

(A) 1. **(B)** no change.

(C) 0. **(D)** high impedance.

Ans: C

J=0, K=1, these inputs will reset the flip-flop after the clock pulse. So whatever be the previous output, the next state will be 0.

Q.95 Which of following are known as universal gates

(A) NAND &NOR. **(B)** AND &OR.

(C) XOR&OR. **(D)** None.

Ans: A

NAND & NOR are known as universal gates, because any digital circuit can be realized completely by using either of these two gates.

Q.96 Which of the following memories stores the most number of bits

(A) 64K×8 memory. **(B)** 1M ×8 memory.

(C) 32M ×8memory. **(D)** 64 × 6memory.

Ans: C

32M x 8 stores most number of bits

$2^5 \times 2^{20}=2^{25}$ $(1M = 2^{20} = 1K \times 1K = 2^{10} \times 2^{10})$

Q.97 Which of following consume minimumpower

(A) TTL. **(B)**CMOS.

(C)DTL. **(D)**RTL.

Ans: B

CMOS consumes minimum power as in CMOS one p-MOS & one n-MOS transistors are connected in complimentary mode, such that one device is ON & one is OFF.

Q.98 In the decimal numbering system, what is theMSD?

a. the middle digit of a stream of numbers

B. the digit to the right of the decimal point

c. the last digit on the right

d. the digit with the most weight

Ans: D

The digit with the most weight

Q.99 Which of the following statements does NOT describe an advantage of digitaltechnology?

a. the values may vary over a continuousrange.

b. the circuits are less affected bynoise.

c. the operation can beprogrammed.

d. information storage iseasy.

Ans: A

a. the values may vary over a continuous range.

Q.100 The generic array logic (GAL)deviceis_____.

a. one-timeprogrammable

b. reprogrammable

c. a cmosdevice

d. reprogrammable and a cmos device

Ans : B

b. reprogrammable